# Analysis of Queueing Displacement Using Switch Port Speedup* 

Israel Cidon ${ }^{\dagger}$<br>Department of Electrical Engineering<br>Technion - Israel Institute of Technology<br>Haifa 32000, Israel<br>cidon@ee.technion.ac.il

Asad Khamisy<br>SUN Microsystems Labs<br>2550 Garcia Avenue<br>Mountain View, CA 94043, U.S.A.<br>asad@eng.sun.com

Moshe Sidi ${ }^{\ddagger}$<br>Department of Electrical Engineering<br>Technion - Israel Institute of Technology<br>Haifa 32000, Israel<br>moshe@ee.technion.ac.il


#### Abstract

Current high-speed packet switching systems, ATM in particular, have large port buffering requirements. The use of highly integrated ASIC technology for implementing high-degree and high-speed switch fabrics is facing a technology mismatch in the sense that today's chip technology does not allow to integrate on-chip the high-speed switching fabric with the large buffering requirements. Consequently, many designs are based on the principles of queueing displacement, i.e., they attempt to move the queueing point off-chip. This is usually done by considerably speeding-up the on-chip switch output ports and placing a second external stage of buffering between the switch fabric and the outgoing link circuitry. Such designs are very popular and are used by many current $A T M$ switch vendors. While such schemes are widely used, no rigorous analysis has so far been offered to evaluate the design trade-offs and to quantify the design points.

The model we use to analyze the performance of the above system is a two-node tandem queueing system. The first node in the tandem corresponds to the internal buffer while the second node in the tandem corresponds to the external buffer. It is assumed that the internal buffer is capable to transfer $c_{1}$ cells per time unit to the external buffer, while the external buffer is served at a lower rate of $c_{2}$ cells per time unit.


[^0]
## 1 Introduction

This paper addresses basic design and performance issues in the architecture of hardware based fast packet switches. The ability to implement cost-effective high-speed switches in silicon is (along with the advance of fiber-optic technologies) the enabling technology behind the recent rise of broadband integrated networks, in particular the ATM architecture $[1,2,3,4,5,6]$. Fast hardware based switches have also been at the core of the emerging switched LAN (also termed switching hubs) products as well as the new generation of Gigabit routers [www.bbn.com/magazine/techwatch/router.html].

Current switching system designs in high-speed packet-switching networks and in particular the emerging ATM market have large and consistently growing port buffering requirements. This trend follows the expected use of ATM networks for bursty data applications, the use of reactive flow control over ever increasing link speeds and the separation of different QoS classes and connection groups to dedicated buffers. While in the past ATM vendors have frequently offered switches with less than a hundred cell (5Kbytes) buffers, the numbers today have grown typically to more than 10K cell buffers. These numbers are expected to continue to grow with the speed of links, with the geographical distances, as well as with the use of more sophisticated buffer scheduling mechanisms. For example, Fore System [www.fore.com/html/products/datasheets/2famcamp. html] advertises buffer sizes of 53 K cells (almost 3 Mbytes ) and 212 K cells (11Mbytes) for its ASX200 and ASX-1000 ATM switches, respectively.

Cisco [www.cisco.com/warp/public/641/16.html] advertises 64 K cells output buffers per link for its LightStream 2020 ATM switch. Stratacom provides 64 K cells per port at its BPX switch [www.stratacom.com/products/bpxaxis.html]. The GTE [www.gte.com/Cando/Carrier/Docs/Wired/ span4000.html] SPANet 4000 ATM switch is designed with a buffer size of 16 K cells.

Most hardware based switch designs rely on the new generation of CMOS ASICs which are very popular within products which require fast turn-around and at the same time high integration and high performance. (Nevertheless, these following statements are also correct for today's fully custom VLSI designs.) The use of highly integrated ASIC technology for implementing high-degree and high-speed switch fabrics ( 8 X 8 to 32 X 32 with $155-622 \mathrm{Mbps}$ ) is facing a technology mismatch in the sense that today's technology does not allow to integrate within the same ASIC the high-speed switching fabric logic of many ports with the large amount of fast memory required to buffer all switch output ports.


Figure 1: Speedup used to extend the memory in an ASIC based switch

Consequently, many designs are based on the principles of queueing displacement, i.e., the attempt to move the queueing point off-chip and implement the main buffer using standard RAM technology. This is usually done by considerably speeding-up the integrated switch output ports (compared to the actual link speed supported) and placing a second stage (external to the switch) of buffering between the switch fabric and the outgoing link. The much higher speed at which the internal buffer is off-loaded, considerably reduces its memory requirements for a given overflow probability design point. Such a design is very popular and is used by many current

ATM switch vendors (usually termed as speedup). In particular, the ones which base their buffering design on output queueing techniques. (Other designs are also possible, for example, pure input queueing or a shared memory design based exclusively on off-the-shelf RAM.) Figure 1 depicts an ASIC with a limited on-chip buffer at the switching fabric being extended with an external memory using the speedup technique. For example, the IBM switch-on-a-chip Prizma chip is limited by the number of on-chip buffers and employs speedup technique [www.zurich.ibm.com/Technology/ATM/SWOCPWP] and [8]. Bay Networks, uses speedup in its Lattice Cell switch design to increase the effective amount of buffers in its multi-stage switching fabric.

While speedup schemes are widely used, no rigorous analysis has so far been offered to evaluate the design trade-offs and to quantify the design points. The designer would like to evaluate the size of the internal and external buffers required for a certain design point as well as the speed of the path connecting them together. In particular, it is attractive to map (or lower bound) such dual stage designs to the performance of an "ideal" output queueing design in order to be able to compare different switches of different design points. The following works have addressed the speedup problem or have used queueing models which are related to our problem. In [10], the speedup effect was explored using a tandem system model composed of an $M / M / C$ queue feeding a dependent $M / M / 1$ queue. This model was investigated by extensive simulation and no rigorous analysis was carried out for the speedup problem. In the relevant tandem queues models only limited results are available. In [9] a tandem of two single server discrete-time queues with independent and identically distributed external arrival processes, where the output of one queue is fed as an additional input for the other queue is solved. This is a special case of our solution when no speedup exists and the server can serve only a single cell at a time slot. In [11, 12] Boxma analyzes two exponential single server queues in series where the first queue has a Poisson arrival process and the second is fed by the output of the first. In both queues the same customers have the same service times. In this case, again, the system in question has no speedup. In [13] a tandem of multiple queues in which message sizes are preserved is considered. Several properties of the joint work load distribution (but no full solution) are presented and proved for such a system.

The model we use to analyze the performance of the system with speed-up is a two-node tandem discrete-
time queueing system. The first node in the tandem corresponds to the internal (in-ASIC) buffer while the second node in the tandem corresponds to the external buffer. We begin the analysis of this system assuming that the external buffer can output at most one cell per slot and derive the generating function of the joint probability distribution of the lengths of the two buffers. Moments of the queue lengths are then derived. In addition, we introduce an explicit recursion to compute the joint probability distribution. From this we are able to compute tail probabilities that enable us to dimension the length of the buffers required to guarantee small loss probabilities when the buffers are finite. Speedup of two has special implementation importance as it is a very common and convenient speedup to design and use. It usually does not require tricky clock resynchronizations as either one clock is derived from the other or the path that connects the two buffer stages is of double width. Intuitively, with such speedup, the load on the first buffer stage is only half the load on the output port. In a well controlled network, no link should be overloaded (on the average) and hence the first port has a load limitation of 0.5 . This rather low load should enable us to use very few buffers at the internal first stage. Our main numerical conclusion supports this intuition and shows that the internal buffer can be kept small without damaging the performance of the whole system. We extend the analysis to more general models in which the external buffer can output several cells per slot, and again obtain the generating function of the joint probability distribution of the lengths of the two buffers and the moments. The conclusions obtained are similar to the above.

## 2 The Model

The model we use to analyze the performance of the system with speed-up is a two-node tandem discretetime queueing system. The first node in the tandem corresponds to the internal (in-ASIC) buffer while the second node in the tandem corresponds to the external buffer. Time is slotted into fixed size slots. It is assumed that during each slot the internal buffer is capable to transfer $c_{1}$ cells to the external buffer, while the external buffer is capable to output from the system $c_{2}$ cells. Since the internal buffer is faster than the external buffer, $c_{1}>c_{2}$. Note that when $c_{2}=1$ we have integral speedups ( $c_{1}: 1$ ), while for a general $c_{2}$ we can have any rational speedup $\left(c_{1}: c_{2}\right)$.

Let $A_{1}^{(n)}$ and $A_{2}^{(n)}$ be the number of new cells arriving (from outside the system) during slot $n$ to the first node and the second node, respectively. The arrival process of these new cells at the system is
assumed to be an independent and identically distributed (in each slot) process, namely, $\left\{A_{1}^{(n)}, A_{2}^{(n)}\right\}$ is independent of $\left\{A_{1}^{(k)}, A_{2}^{(k)}\right\}$ for any $n \neq k$, and $\operatorname{Prob}\left(A_{1}^{(n)}=i, A_{2}^{(n)}=j\right)=a_{i, j}$ is independent of n. Let $A\left(z_{1}, z_{2}\right)=\sum_{i=0}^{\infty} \sum_{j=0}^{\infty} a_{i, j} z_{1}^{i} z_{2}^{j}$ be the joint generating function of the arrival processes to the two nodes. Note that arrivals to the two buffers in the same slot may be correlated. We let $r_{l}=$ $\sum_{i_{1}=0}^{\infty} \sum_{i_{2}=0}^{\infty} i_{l} a_{i_{1}, i_{2}}=\partial A\left(z_{1}, z_{2}\right) /\left.\partial z_{l}\right|_{z_{1}=z_{2}=1}$ be the arrival rate of cells to node $l(l=1,2)$. For the sake of the analysis, we assume that both buffers are of infinite size. We will later discuss how this assumption can be dealt with to attain the performance of realistic switches. (Note that the speedup based output port system corresponds to the case with no external arrivals to the second node, i.e., $a_{i, j}=0, j>0$.)

## 3 Analysis

We begin our analysis with $c_{2}=1$, namely, a single cell can be transmitted by the second node and leave the system during a slot. Note that when $c_{1}=1$, our system is identical to the system analyzed in [9]. In our analysis we are interested in computing the steadystate probabilities of the lengths of the two nodes. Since at most one cell can leave the system during a slot, steady-state exists if $r_{1}+r_{2}<1$.

Assume that departures take place at the end of slots and arrivals within slots. Let $Q_{1}^{(n)}$ and $Q_{2}^{(n)}$ denote the lengths of the first node and the second node at the end of slot $n$, respectively. Let $p_{i, j}^{(n)}=\operatorname{Prob}\left(Q_{1}^{(n)}=i, Q_{2}^{(n)}=j\right)$ and $G^{(n)}\left(z_{1}, z_{2}\right)=\sum_{i=0}^{\infty} \sum_{j=0}^{\infty} p_{i, j}^{(n)} z_{1}^{i} z_{2}^{j}$ be the generating function of the joint queue length distribution at both nodes. We let $p_{i, j}=\lim _{n \rightarrow \infty} p_{i, j}^{(n)}$ and $G\left(z_{1}, z_{2}\right)=$ $\lim _{n \rightarrow \infty} G^{(n)}\left(z_{1}, z_{2}\right)$.

The evolution equation of the queue lengths for $n \geq$ 0 is given by

$$
\begin{align*}
Q_{1}^{(n+1)}= & \left(Q_{1}^{(n)}-c_{1}\right)^{+}+A_{1}^{(n)} \\
Q_{2}^{(n+1)}= & \left(Q_{2}^{(n)}-1\right)^{+} \\
& +\min \left(Q_{1}^{(n)}, c_{1}\right)+A_{2}^{(n)} \tag{1}
\end{align*}
$$

From which we have in steady-state $(n \rightarrow \infty)$,

$$
\begin{aligned}
& G\left(z_{1}, z_{2}\right)=A\left(z_{1}, z_{2}\right)\left\{p_{0,0}+\sum_{i=1}^{c_{1}-1} p_{i, 0} z_{1}^{i} \cdot z_{1}^{-i} z_{2}^{i}\right. \\
& \quad+\sum_{i=1}^{c_{1}-1} \sum_{j=1}^{\infty} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-i} z_{2}^{i-1} \\
& \quad+\sum_{j=1}^{\infty} p_{0, j} z_{2}^{j} \cdot z_{2}^{-1}+\sum_{i=c_{1}}^{\infty} p_{i, 0} z_{1}^{i} \cdot z_{1}^{-c_{1}} z_{2}^{c_{1}}
\end{aligned}
$$

$$
\begin{equation*}
\left.+\sum_{i=c_{1}}^{\infty} \sum_{j=1}^{\infty} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-c_{1}} z_{2}^{c_{1}-1}\right\} \tag{2}
\end{equation*}
$$

Simple algebraic manipulations yield the following,

$$
\begin{equation*}
G\left(z_{1}, z_{2}\right)=A\left(z_{1}, z_{2}\right) \frac{B\left(z_{1}, z_{2}\right)}{z_{1}^{c_{1}} z_{2}-z_{2}^{c_{1}} A\left(z_{1}, z_{2}\right)} \tag{3}
\end{equation*}
$$

where $B\left(z_{1}, z_{2}\right)=\sum_{i=0}^{c_{1}-1}\left[p_{i, 0}\left(z_{2}-1\right)+g_{i}\left(z_{2}\right)\right]\left(z_{1}^{c_{1}} z_{2}^{i}-\right.$ $\left.z_{1}^{i} z_{2}^{c_{1}}\right)+G\left(z_{1}, 0\right) z_{2}^{c_{1}}\left(z_{2}-1\right)$ and $g_{i}\left(z_{2}\right)=\frac{1}{i!} \frac{\partial G^{i}\left(z_{1}, z_{2}\right)}{\partial z_{1}^{i}}$ at $z_{1}=0$.

In (3), we encounter a common phenomenon in dependent queues, namely, that the generating functions $G\left(z_{1}, z_{2}\right)$ is expressed in terms of several boundary functions. In order to uniquely determine $G\left(z_{1}, z_{2}\right)$ we will have to determine the boundary functions, $G\left(z_{1}, 0\right)$ and $g_{i}\left(z_{2}\right), 0 \leq i \leq c_{1}-1$. In what follows, we develop the method for obtaining these boundary functions. Along this process we mainly use the analytic properties of the generating functions $G\left(z_{1}, z_{2}\right)$ in the disk $\left|z_{i}\right|<1, \quad i=1,2$.

We begin by letting $z_{2} \rightarrow 0$ in (2) to obtain $G\left(z_{1}, 0\right)=A\left(z_{1}, 0\right)\left[p_{0,0}+p_{0,1}\right]$. When $z_{1}=0$ we have that

$$
\begin{equation*}
p_{0,0}=a_{0,0}\left(p_{0,0}+p_{0,1}\right) \tag{4}
\end{equation*}
$$

Therefore we can express $G\left(z_{1}, 0\right)$ (and the corresponding probabilities $p_{i, 0}, i \geq 1$ ) in terms of the constant $p_{0,0}$ as follows,

$$
\begin{equation*}
G\left(z_{1}, 0\right)=A\left(z_{1}, 0\right) \frac{p_{0,0}}{a_{0,0}} ; \quad p_{i, 0}=a_{i, 0} \frac{p_{0,0}}{a_{0,0}} i \geq 1( \tag{5}
\end{equation*}
$$

To determine $g_{i}\left(z_{2}\right), 0 \leq i \leq c_{1}-1$, we use the fact that for any $\left|z_{2}\right|<1$, the denominator $z_{1}^{c_{1}} z_{2}-z_{2}^{\epsilon_{1}} A\left(z_{1}, z_{2}\right)$ of (3) has exactly $c_{1}$ roots within the unit disk $\left|z_{1}\right|<1$ (the proof is based on Rouche's Theorem). Let these roots be denoted by $\sigma_{l}\left(z_{2}\right), 1 \leq$ $l \leq c_{1}$. Since $G\left(z_{1}, z_{2}\right)$ is an analytic function in the disk $\left|z_{i}\right|<1, \quad i=1,2$, the nominator of (3) must vanish at each of these roots, i.e.,

$$
\begin{equation*}
B\left(\sigma_{l}\left(z_{2}\right), z_{2}\right)=0 \quad, \quad 1 \leq l \leq c_{1} \tag{6}
\end{equation*}
$$

where in the above we use $p_{i, 0}$ from (5) and $G\left(\sigma_{l}\left(z_{2}\right), 0\right)=A\left(\sigma_{l}\left(z_{2}\right), 0\right) p_{0,0} / a_{0,0} . \quad$ Expression (6) is a set of $c_{1}$ (linear) equations that determines the functions $g_{i}\left(z_{2}\right), 0 \leq i \leq c_{1}-1$ up to the constant $p_{0,0}$.

To complete the derivation of the generating function we need to compute that constant. To that end, let $z_{1}=z_{2}=z$ in (3) to obtain,

$$
\begin{align*}
G(z, z) & =A(z, z) \frac{G(z, 0)(z-1)}{z-A(z, z)} \\
& =A(z, z) \frac{A(z, 0) p_{0,0}(z-1)}{a_{0,0}[z-A(z, z)]} \tag{7}
\end{align*}
$$

Letting $z \rightarrow 1$ in the above and assuming that the steady-state condition $r_{1}+r_{2}<1$ holds, we obtain by using L'Hôpital's law,

$$
\begin{equation*}
p_{0,0}=\frac{a_{0,0}\left(1-r_{1}-r_{2}\right)}{A(1,0)} \tag{8}
\end{equation*}
$$

This completes the derivation of the joint generating function of the queue-length probability distribution.

Using the generating function we can obtain the average number of cells in node $i(i=1,2)$, denoted by $L_{i}$. Letting $z_{2}=1$ in (3) we have

$$
G\left(z_{1}, 1\right)=A\left(z_{1}, 1\right) \frac{\sum_{i=0}^{c_{1}-1} g_{i}(1)\left(z_{1}^{c_{1}}-z_{1}^{i}\right)}{z_{1}^{e_{1}}-A\left(z_{1}, 1\right)}
$$

Taking the derivative of the above expression with respect to $z_{1}$ and letting $z_{1} \rightarrow 1$ we obatin,

$$
\begin{equation*}
L_{1}=r_{1}+\frac{\sum_{i=0}^{c_{1}-1} g_{i}(1)\left(c_{1}^{2}-i^{2}\right)+r_{1}-c_{1}^{2}+\hat{A}}{2\left(c_{1}-r_{1}\right)} \tag{9}
\end{equation*}
$$

where $\hat{A}=d^{2} A(z, 1) /\left.d z^{2}\right|_{z=1}$.
Taking the derivative of (7) with respect to $z$ and letting $z \rightarrow 1$ we obatin (using (8)),

$$
\begin{equation*}
L_{1}+L_{2}=r_{1}+r_{2}+\left.\frac{d A(z, 0)}{d z}\right|_{z=1}+\frac{\left.\frac{d^{2} A(z, z)}{d z^{2}}\right|_{z=1}}{2\left(1-r_{1}-r_{2}\right)}(1 \tag{10}
\end{equation*}
$$

Subtracting (9) from (10) we obtain the average number of cells in the second node $L_{2}$.

## 4 The Probability Distribution

The joint generating function derived in the previous section allows us to compute $p_{0,0}$ and the average quantities easily. However, the computation of the probabilities themselves is difficult. In this section we develop a recursion for the computation of the steadystate probabilities $p_{n_{1}, n_{2}}$. From equation (4) we obtain $p_{0,1}=p_{0,0}\left(1-a_{0,0}\right) / a_{0,0}$. Together with equations (5) and (8) we have the initial conditions for the recursion, i.e., we know $p_{i, 0}, i \geq 0$ and $p_{0,1}$.

Next, we compute the probabilities $p_{n_{1}, n_{2}}$ for $n_{1} \geq$ 0 and $1 \leq n_{2} \leq c_{1}-1$ (except for $p_{0,1}$ that is known already). In order to have $n_{2}, 1 \leq n_{2} \leq c_{1}-1$, cells in the second queue, the number of cells in the first queue at the end of the previous slot have to be less or equal to $n_{2}$. Assume the number of cells in the first queue is $i, 0 \leq i \leq c_{1}-1$, then in order to have $n_{1}$ cells in the first queue, all $n_{1}$ cells have to arrive from the external source. Further, assuming that $j$ cells arrive to the second queue from the external source,
the total number of cells that arrive to the second queue is $i+j$. If the second queue is not empty at the end of the previous slot, then in order to have $n_{2}$ cells, the number of cells at the end of the previous slot have to be $n_{2}+1-i-j$, where the plus 1 accounts for the cell that must have departed the second queue. We have for $n_{1} \geq 0,1 \leq n_{2} \leq c_{1}-1$ that

$$
\begin{align*}
p_{n_{1}, n_{2}} & =\sum_{i=0}^{n_{2}} p_{i, 0} a_{n_{1}, n_{2}-i} \\
& +\sum_{i=0}^{n_{2}} \sum_{j=0}^{n_{2}-i} p_{i, n_{2}+1-i-j} a_{n_{1}, j} \tag{11}
\end{align*}
$$

where the first sum corresponds to the case where the second queue is empty at the end of the previous slot. Note that $n_{1}$ appears in the right hand side of equation (11) only in $a_{n_{1}, l}$ for some $l$ (and does not appear in any of the $p$ 's). In equation (11) we compute the probabilities $p_{n_{1}, n_{2}}$ in increasing order of $n_{2}$ as follows. We assume that $p_{i, j}$ for $i \geq 0,0 \leq j \leq n_{2}-2$ as well as $p_{0, n_{2}-1}$ are known (initially, for $n_{2}=2$ this is true as explained at the beginning of this section). Next, we compute $p_{0, n_{2}}, p_{1, n_{2}-1}$ by solving two equations with two unknowns. These equations correspond to equation (11) with $p_{0, n_{2}-1}$ and $p_{1, n_{2}-1}$ in the left hand side. Note that the unknown $p_{0, n_{2}}$ appears only in the right hand side of (11), while the unknown $p_{1, n_{2}-1}$ appears also in the left hand side. After some simple algebra we obtain the solution for $p_{0, n_{2}}, p_{1, n_{2}-1}$ as,

$$
\begin{align*}
p_{0, n_{2}} & =\left(\beta_{1, n_{2}}(1) a_{0,0}-\beta_{1, n_{2}}(0)\left(a_{1,0}-1\right)\right) / a_{0,0} \\
p_{1, n_{2}-1} & =\left(\beta_{1, n_{2}}(0) a_{1,0}-\beta_{1, n_{2}}(1) a_{0,0}\right) / a_{0,0} \quad(12) \tag{12}
\end{align*}
$$

where we define

$$
\begin{align*}
& \beta_{1, n_{2}}(l) \triangleq 1\{l=0\} p_{0, n_{2}-1} \\
& -\sum_{i=0}^{\min \left(c_{1},\left(n_{2}-1\right)\right)} \sum_{j=1}^{n_{2}-i} p_{i, n_{2}-i-j} a_{l, j-1\left\{j=n_{2}-i\right\}} \\
& -\sum_{i=2}^{\min \left(c_{1},\left(n_{2}-1\right)\right)} p_{i, n_{2}-i} a_{l, 0} \quad l=0,1
\end{align*}
$$

Now the probabilities $p_{n_{1}, n_{2}-1}$ for $n_{1} \geq 2$ are computed directly from equation (11). Recursing this procedure completes the computation of the probabilities $p_{n_{1}, n_{2}}$ for $n_{1} \geq 0$ and $1 \leq n_{2} \leq c_{1}-1$.

Next, we compute the probabilities $p_{n_{1}, n_{2}}$ for $n_{1} \geq$ 0 and $n_{2} \geq c_{1}$. There are two cases to consider in the recursion, the first is when the number of cells in the first queue is less than $c_{1}$ in which case all cells move to the second queue, and the case where the number of cells in the first queue is greater or equal to $c_{1}$ in
which case only $c_{1}$ cells move from the first queue to the second queue. Similar to the previous recursion, we have for $n_{1} \geq 0, n_{2} \geq c_{1}$,

$$
\begin{aligned}
p_{n_{1}, n_{2}} & =\sum_{i=0}^{c_{1}-1} p_{i, 0} a_{n_{1}, n_{2}-i} \\
& +\sum_{i=0}^{c_{1}-1} \sum_{j=0}^{n_{2}-i} p_{i, n_{2}+1-i-j} a_{n_{1}, j} \\
& +\sum_{i=c_{1}}^{n_{1}+c_{1}} p_{i, 0} a_{n_{1}+c_{1}-i, n_{2}-c_{1}} \\
& +\sum_{i=c_{1}}^{n_{1}+c_{1}} \sum_{j=0}^{n_{2}-c_{1}} p_{i, n_{2}+1-c_{1}-j} a_{n_{1}+c_{1}-i, \chi}(14)
\end{aligned}
$$

In the same way as before, we write two equations for $p_{0, n_{2}-1}$ and $p_{1, n_{2}-1}$, from which we obtain the probabilities $p_{0, n_{2}}, p_{1, n_{2}-1}$. Then we use equation (14) to compute the probabilities $p_{n_{1}, n_{2}-1}$ for $n_{1} \geq 2$. The solution for $p_{0, n_{2}}, p_{1, n_{2}-1}$ in this case is given by:

$$
\begin{align*}
p_{0, n_{2}} & =\left(\beta_{2, n_{2}}(1) a_{0,0}-\beta_{2, n_{2}}(0)\left(a_{1,0}-1\right)\right) / a_{0,0} \\
p_{1, n_{2}-1} & =\left(\beta_{2, n_{2}}(0) a_{1,0}-\beta_{2, n_{2}}(1) a_{0,0}\right) / a_{0,0} \tag{15}
\end{align*}
$$

Where we define $\beta_{2, n_{2}}(0) \triangleq \beta_{1, n_{2}}(0)$ and $\beta_{2, n_{2}}(1)$

$$
\triangleq \beta_{1, n_{2}}(1)+\sum_{j=0}^{n_{2}-c_{1}} p_{c_{1}+1, n_{2}-c_{1}-j} a_{0, j-1\left\{j=n_{2}-c_{1}\right\}}
$$

Now the probabilities $p_{n_{1}, n_{2}-1}$ for $n_{1} \geq 2$ are computed directly from equation (14). This completes the computation of the probabilities $p_{n_{1}, n_{2}}$ for $n_{1} \geq 0$ and $n_{2} \geq c_{1}$.

The computation complexity of the probabilities $p_{n_{1}, n_{2}}$ for $0 \leq n_{1} \leq N_{1}$ and $0 \leq n_{2} \leq N_{2}$ is in the order of $O\left(N_{1}^{2} N_{2}^{2}\right)$.

### 4.1 Overflow Probability

Since we use infinite buffers in our model, we approximate the cell loss probability by the buffer overflow probability. The first (second) node is in overflow state when the number of cells in the buffer exceeds $N_{1}\left(N_{2}\right)$.

If the state upon arrival is $\left(n_{1}, n_{2}\right)$, then the the number of cells in the second queue in front of this cell, when this cell arrives to the second queue, will be $n_{1}+n_{2}-\sum_{i=1}^{\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil} A_{2}(i)-\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil$, where $A_{2}(i)$ denotes the number of cells that arrive to the second queue in slot number $i$ (the slot of arrival of the cell is marked as slot number 1). This is true since 1. The cell will arrive at the second queue $\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil$ slots after it arrived to the system, and 2. $c_{1}>1$ and hence the second queue will not empty in the next $\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil$ slots after the arrival of this cell.

Correspondingly, we define the overflow probability in the system as the probability that the number of
cells in the first and second nodes at slot boundaries fulfil the relation $\left(n_{1}, n_{2}\right) \in\left\{\left(n_{1}, n_{2}\right) \mid n_{1}>N_{1}, n_{1}+\right.$ $\left.n_{2}-\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil>N_{2}\right\}$.

Next, we consider a system without external arrivals to the second queue, i.e., $a_{i, j}=0, j>0$. Then, the overflow probability in the system is equal to

$$
\begin{equation*}
P_{\text {over flow }}=1-\sum_{n_{1}=0}^{N_{1}} \sum_{n_{2}=0}^{N_{2}+\left\lceil\left(n_{1}+1\right) / c_{1}\right\rceil-n_{1}} p_{n_{1}, n_{2}} \tag{16}
\end{equation*}
$$

## 5 The case $c_{2}>1$

We now consider a system with $c_{2}>1$, namely, several cells $\left(c_{2}\right)$ can be transmitted by the second node and leave the system during a slot. As before, we are interested in computing the steady-state probabilities of the lengths of the two nodes. Since $c_{2}>1$ cells can leave the system during a slot, steady-state exists if $r_{1}+r_{2}<c_{2}$.

With the same notations as in Section 3 the evolution equation of the queue lengths for $n \geq 0$ is given by

$$
\begin{align*}
Q_{1}^{(n+1)}= & \left(Q_{1}^{(n)}-c_{1}\right)^{+}+A_{1}^{(n)} \\
Q_{2}^{(n+1)}= & \left(Q_{2}^{(n)}-c_{2}\right)^{+} \\
& +\min \left(Q_{1}^{(n)}, c_{1}\right)+A_{2}^{(n)} \tag{17}
\end{align*}
$$

Similar to the method for obtaining (2), we obtain in this case,

$$
\begin{align*}
G\left(z_{1}, z_{2}\right) & =A\left(z_{1}, z_{2}\right)\left\{\sum_{i=0}^{c_{1}-1} \sum_{j=0}^{c_{2}-1} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-i} z_{2}^{i-j}\right. \\
& +\sum_{i=0}^{c_{1}-1} \sum_{j=c_{2}}^{\infty} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-i} z_{2}^{i-c_{2}} \\
& +\sum_{i=c_{1}}^{\infty} \sum_{j=0}^{c_{2}-1} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-c_{1}} z_{2}^{c_{1}-j} \\
& \left.+\sum_{i=c_{1}}^{\infty} \sum_{j=c_{2}}^{\infty} p_{i, j} z_{1}^{i} z_{2}^{j} \cdot z_{1}^{-c_{1}} z_{2}^{c_{1}-c_{2}}\right\} \tag{18}
\end{align*}
$$

and after simple algebraic manipulations we get,

$$
\begin{equation*}
G\left(z_{1}, z_{2}\right)=A\left(z_{1}, z_{2}\right) \frac{B\left(z_{1}, z_{2}\right)}{z_{1}^{c_{1}} z_{2}^{c_{2}}-z_{2}^{c_{1}} A\left(z_{1}, z_{2}\right)} \tag{19}
\end{equation*}
$$

where $B\left(z_{1}, z_{2}\right)=\sum_{i=0}^{c_{1}-1}\left[\sum_{j=0}^{c_{2}-1} p_{i, j}\left(z_{2}^{c_{2}}\right.\right.$
$\left.\left.z_{2}^{i}\right)+g_{i}\left(z_{2}\right)\right]\left(z_{1}^{c_{1}} z_{2}^{i}-z_{1}^{i} z_{2}^{c_{1}}\right)+\sum_{j=0}^{c_{2}-1} f_{j}\left(z_{1}\right) z_{2}^{c_{1}}\left(z_{2}^{c_{2}}-z_{2}^{j}\right)$ and
$g_{i}\left(z_{2}\right)=\left.\frac{1}{i!} \frac{\partial G^{i}\left(z_{1}, z_{2}\right)}{\partial z_{1}^{i}}\right|_{z_{1}=0}, f_{j}\left(z_{1}\right)=\left.\frac{1}{j!} \frac{\partial G^{j}\left(z_{1}, z_{2}\right)}{\partial z_{2}^{j}}\right|_{z_{2}=0}$. In order to uniquely determine $G\left(z_{1}, z_{2}\right)$ we will have to determine the boundary functions, $f_{j}\left(z_{1}\right), 0 \leq j \leq$ $c_{2}-1$ and $g_{i}\left(z_{2}\right), 0 \leq i \leq c_{1}-1$. In what follows, we demonstrate the method for obtaining these boundary functions. Along this process we mainly use the analytic properties of the generating functions $G\left(z_{1}, z_{2}\right)$ in the disk $\left|z_{i}\right|<1, \quad i=1,2$.

We begin by taking the $l$-th derivative ( $0 \leq l \leq$ $c_{2}-1$ ) of both sides of (18) with respect to $z_{2}$ and let $z_{2} \rightarrow 0$ to obtain,

$$
\begin{equation*}
f_{l}\left(z_{1}\right)=\sum_{k=0}^{l} \frac{\mathcal{A}_{l-k}\left(z_{1}\right) u_{k}}{(l-k)!} \tag{20}
\end{equation*}
$$

where $\mathcal{A}_{i}\left(z_{1}\right)=\partial A^{i}\left(z_{1}, z_{2}\right) /\left.\partial z_{2}^{i}\right|_{z_{2}=0}$, and $u_{k}=$ $\sum_{j=0}^{c_{2}} p_{k, j}+\sum_{j=0}^{k-1} p_{j, c_{2}+k-j}$.

Consequently, $f_{l}\left(z_{1}\right)$ (and the corresponding probabilities $p_{i, l}, i \geq 0$ ) are expressed in terms of the constants $u_{k}, 0 \leq k \leq l$. To determine these constants, we let $z_{1}=z_{2}=z$ in (19) to obtain,

$$
\begin{equation*}
G(z, z)=A(z, z) \frac{\hat{B}(z)}{z^{c_{2}}-A(z, z)} \tag{21}
\end{equation*}
$$

where $\hat{B}(z)=\sum_{j=0}^{c_{2}-1}\left(z^{c_{2}}-z^{j}\right) \sum_{k=0}^{j} \mathcal{A}_{j-k}(z) u_{k} /(j-$ $k)$ !. Letting $z \rightarrow 1$ in the above and assuming that the steady-state condition $r_{1}+r_{2}<c_{2}$ holds, we obtain

$$
\begin{equation*}
c_{2}-r_{1}-r_{2}=\sum_{j=0}^{c_{2}-1}\left(c_{2}-j\right) \sum_{k=0}^{j} \frac{\mathcal{A}_{j-k}(1) u_{k}}{(j-k)!} \tag{22}
\end{equation*}
$$

Furthermore, the denominator $z^{c_{2}}-A(z, z)$ of (21) has one root at $z=1$ and exactly $c_{2}-1$ roots within the unit disk $|z|<1$ (the proof is based on Rouche's Theorem). Let these roots be denoted by $\mu_{l}, 1 \leq l \leq$ $c_{2}-1$. Since $G(z, z)$ is an analytic function in the disk $|z|<1$, the nominator of (21) must vanish at each of these roots, i.e., for $1 \leq l \leq c_{2}-1$,

$$
\begin{equation*}
\sum_{j=0}^{c_{2}-1}\left(\mu_{l}^{c_{2}}-\mu_{l}^{j}\right) \sum_{k=0}^{j} \frac{\mathcal{A}_{j-k}\left(\mu_{l}\right) u_{k}}{(j-k)!}=0 \tag{23}
\end{equation*}
$$

Equation (22) together with (23) is a set of $c_{2}$ (linear) equations that determines the constants $u_{k}, 0 \leq k \leq$ $c_{2}-1$, and hence the boundary functions $f_{j}\left(z_{1}\right), 0 \leq$ $j \leq c_{2}-1$ are determined (using (20)). From $f_{j}\left(z_{1}\right)$ we can obtain $p_{i, j}, j \geq 0$ by taking the $i$-th derivative of $f_{j}\left(z_{1}\right)$ with respect to $z_{1}$ and letting $z_{1} \rightarrow 0$.

To determine $g_{i}\left(z_{2}\right), 0 \leq i \leq c_{1}-1$, we use the same procedure described in Section 3. In particular, we note that for any $\left|z_{2}\right|<1$, the denominator $z_{1}^{c_{1}} z_{2}^{c_{2}}-$ $z_{2}^{c_{1}} A\left(z_{1}, z_{2}\right)$ of (19) has exactly $c_{1}$ roots within the
unit disk $\left|z_{1}\right|<1$ (the proof is based on Rouche's Theorem). Let these roots be denoted by $\sigma_{l}\left(z_{2}\right), 1 \leq$ $l \leq c_{1}$. Since $G\left(z_{1}, z_{2}\right)$ is an analytic function in the disk $\left|z_{i}\right|<1, \quad i=1,2$, the nominator of (19) must vanish at each of these roots, i.e.,

$$
\begin{equation*}
B\left(\sigma_{l}\left(z_{2}\right), z_{2}\right)=0 \quad 1 \leq l \leq c_{1} \tag{24}
\end{equation*}
$$

Expression (24) is a set of $c_{1}$ (linear) equations that determines the functions $g_{i}\left(z_{2}\right), \quad 0 \leq i \leq c_{1}-1$.

This completes the derivation of the joint generating function of the queue-length probability distribution. In [14] we provide the procedure for computing the joint probability distribution in this case.

Using the generating function we can obtain the average number of cells in node $i(i=1,2)$, denoted by $L_{i}$, as was done in Section 3. In fact, the average number of cells in the first node does not change with $c_{2}$, hence is identical to (9). Taking the derivative of (21) with respect to $z$ and letting $z \rightarrow 1$ we obatin,

$$
\begin{align*}
& L_{1}+L_{2}=r_{1}+r_{2}+\left.\frac{d^{2} A(z, z)}{d z^{2}}\right|_{z=1} \\
& 2\left(c_{2}-r_{1}-r_{2}\right)  \tag{25}\\
&+\frac{\hat{\mathcal{A}}-c_{2}\left(c_{2}-1\right)}{2\left(c_{2}-r_{1}-r_{2}\right)}
\end{align*}
$$

where $\hat{\mathcal{A}}=\sum_{j=0}^{c_{2}-1} \sum_{k=0}^{j} \frac{u_{k}}{(j-k)!}\left\{\left[c_{2}\left(c_{2}-1\right)-j(j-\right.\right.$ 1) $\left.] \mathcal{A}_{j-k}(1)+2\left(c_{2}-j\right) d \mathcal{A}_{j-k}(z) /\left.d z\right|_{z=1}\right\}$. Subtracting (9) from (25) we obtain the average number of cells in the second node $L_{2}$.

## 6 Numerical Results

In the first example cells arrive to the system (through the first node only) according to a Poisson process with rate $\lambda$. We set $c_{1}=2$ and $c_{2}=1$. In Figure 2 we plot the overflow probability in the system versus the internal buffer size for external buffer size of 80 cells and load of $\lambda=0.9$. We also plot the overflow probability in the internal buffer, external buffer and in an "ideal" output buffer switch with $c_{1}=\infty$. From Figure 2 we notice that for internal buffer size greater or equal to 15 , the overflow probability in the system is less than the overflow probability in the "ideal" system. Also, the main contribution to the total overflow probability for small (large) internal buffer sizes comes from the internal (external) overflow probability. Notice that the internal buffer reduces the burstiness of the input process to the external buffer by limiting the maximum number of cells that can arrive to the external buffer to $c_{1}=2$, and hence the overflow probability in the system and in the external buffer is smaller than the overflow probability in the "ideal" system.

We obtained numerical results for different external buffer sizes and loads where the overflow probability in the "ideal" system was kept at $10^{-7}$. In all examples, an internal buffer size between 12 and 14 cells was sufficient to bring the overflow probability in the system below $10^{-7}$. The same phenomena described in Figure 2 were observed in all examples.


Figure 2: Overflow probability versus internal buffer size for load of 0.9 and external buffer size of 80 cells.

More numerical results are provided in Figure 3 where we plot the overflow probability versus the average load for internal buffer size of 15 and external buffer size of 40 . We see again that internal buffer size of 15 is enough to achieve smaller overflow probability in the system compared to the "ideal" system, for average load of 0.75 or larger (for the range of $\geq 10^{-9}$ overflow probability this is the relevant load range). Numerical results for the case $c_{2}>1$ are provided in [14].


Figure 3: Overflow probability versus average load for internal buffer size of 15 and external buffer size of 40 .

We also simulated a system with bursty traffic model that corresponds to VBR traffic class. Here we used three groups of sources. Each group consists of 10 identical sources. Each source corresponds to Interrupted Poisson Process (IPP) model, with sources in the first group having an average ON period of 100 slots and average OFF period of 100 slots. The second and third group sources have average (ON, OFF) periods of $(100,300)$ and $(100,900)$, respectively. The average load in the system is termed "VBR Load" and the total load of each group is "VBR Load"/3. Table 6 contains the overflow probability in the "ideal" system and in the system versus "VBR Load" for different internal buffer sizes. The conclusions are similar to the Poisson model.
[6] J. Hui, "A broadband packet switch for multirate services," Proc. of International Conference on Comm. (ICC'87): 782-788, June 1987.
[7] AT\&T Microelectronics, Microelectronic Products Selection Guide, AT\&T Microelectronics, Jan. 1995.
[8] W. E. Denzel, A. P. J. Engbersen, I. Iliadis, and G. Karlsson, "A highly modular packet switch for GB/S rates," Proc. of International Switching Symposium, 2:A8.3, Oct. 1992.
[9] J. A. Morrison, "Two discrete-time queues in tandem," IEEE Trans. on Comm., COM-27:563573, 1979.

| VBR Load | Ideal | IB $=8$ | IB $=10$ | IB $=15$ | IB $=20$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0.62 | $2.4210^{-4}$ | $3.0510^{-4}$ | $2.5410^{-4}$ | $2.3810^{-4}$ | $2.3810^{-4}$ |
| 0.66 | $7.1510^{-4}$ | $8.0810^{-4}$ | $7.3110^{-4}$ | $7.0710^{-4}$ | $7.0710^{-4}$ |
| 0.70 | $1.6810^{-3}$ | $1.8110^{-3}$ | $1.7010^{-3}$ | $1.6610^{-3}$ | $1.6610^{-3}$ |
| 0.74 | $3.3510^{-3}$ | $3.5610^{-3}$ | $3.3910^{-3}$ | $3.3110^{-3}$ | $3.3110^{-3}$ |
| 0.78 | $6.0710^{-3}$ | $6.2910^{-3}$ | $6.0910^{-3}$ | $6.0210^{-3}$ | $5.6110^{-3}$ |
| 0.82 | $1.0410^{-2}$ | $1.0610^{-2}$ | $1.0410^{-2}$ | $1.0310^{-2}$ | $1.0310^{-2}$ |

Table 1: Overflow probability versus VBR Load for external buffer size of 100 .

## References

[1] J. S. Turner, "Design of an integrated services packet network," IEEE Journal on Selected Areas in Comm., SAC-4:1373-1380, Nov. 1986.
[2] I. Cidon and I. S. Gopal, "PARIS: An approach to integrated high-speed private networks," International Journal of Digital and Analog Cabled Systems, 1(2):77-85, April 1988.
[3] J. N. Giacopelli and et al, "Sunshine: A high-performance self-routing broadband packet switch architecture," IEEE Journal on Selected Areas in Comm., SAC-9:1289-1298, Oct. 1991.
[4] P. Newman, "A fast packet switch for the integrated services backbone network," IEEE Journal on Selected Areas in Comm., SAC-6:14681479, 1988.
[5] Y. S. Yeh, M. G. Hluchyj, and A. S. Acampora, "The knockout switch: A simple, modular architecture for high performance packet switching," IEEE Journal on Selected Areas in Comm., SAC-5:1274-1283, Oct. 1987.
[10] J. S. C. Chen and T. E. Stern, "Throughput analysis, optimal buffer allocation, and traffic imbalance study of a generic nonblocking packet switch," IEEE Journal on Selected Areas in Comm., SAC-9, 3:439-449, 1991.
[11] O. J. Boxma, "On a tandem queueing model with identical service times at both counters, I," $A d v$. Appl. Prob., (11):616-643, November 1979.
[12] O. J. Boxma, "On a tandem queueing model with identical service times at both counters, II," Adv. Appl. Prob., (11):644-659, November 1979.
[13] S. B. Calo, "Message delays in repeated-service tandem connections," IEEE Trans. on Comm., COM-29:670-678, May 1981.
[14] I. Cidon, A. Khamisy and M. Sidi, "Analysis of Queueing Displacement Using Switch Port Speedup," CC PUB \#170, October 1996.


[^0]:    *The work of I. Cidon and M. Sidi was partially supported by Intel, Israel and by the Fund for the Promotion of Research at the Technion.
    talso with SUN Microsystems Labs, 2550 Garcia Avenue, Mountain View, CA 94043, U.S.A.
    *Part of the work of this author was done while visiting SUN Microsystems Labs, Mountain View CA, U.S.A.

